AMENDMENTS TO THE SPECIFICATION

Paragraph at page 5, line 17:

Fig. 5 is a wave diagram showing voltage levels at floating n-well regions and node [[an In]] A in the I/O buffer; and

Paragraph at page 10, line 10:

When the voltage state at the I/O port 132 is switched from 5V to 0V, the PMOS transistors P2 and P3 are turned off. Further, the inverter INV1 outputs a feedback signal SF to the NMOS transistor N3 according to the input signal of 0V, thus turning on the NMOS transistor N3. The voltage on the node [[an Is]] A is grounded as the NMOS transistors N3 and N4 are turned on. As a result, the system voltage VCC is transferred to the floating N-well region VNW through the PMOS transistor P4, thereby setting the floating N-well VNW at 3.3V. Undesired current leakage is thus prevented.

Paragraph at page 11, line 9:

Fig. 5 is a wave diagram showing the voltage levels at floating N-well region and the node A. Curve Cl shows the voltage level at the floating N-well region in the I/O buffer with feedback control according to the present invention. Curve C2 shows the voltage level at the floating N-well region in the I/O buffer without feedback control. Curve C3 shows the voltage level at node [[an Is]] A is the I/O buffer with feedback control according to the present invention. Curve C4 shows the voltage level at the node [[an Is]] A is the I/O buffer without feedback control. Fig. 6 is a wave diagram showing the voltage levels at the I/O port. Curve C5 shows the voltage level at I/O port in the I/O buffer with feedback control according to the present invention. Curve C6 shows the voltage level at I/O port in the I/O buffer without feedback control. As shown in Figs. 4 and 5, the output signal in the I/O buffer with feedback control according to the present invention drop faster than without feedback control in the output mode. Thus, the present invention provides better output performance than I/O buffers without feedback control.